Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-23. (Canceled)

24. (Currently amended) An apparatus fabricated on a semiconductor substrate ~~for determining a full match for a variable length search key~~, the apparatus comprising:

an embedded processor complex including a plurality of protocol processors and an internal control point processor that ~~provide~~ provides frame processing;

a plurality of hardware accelerator co-processors coupled to the embedded processor complex, wherein the plurality of hardware accelerator co-processors are accessible to each protocol processor and ~~providing~~ provide high speed pattern searching, data manipulation, and frame parsing;

a plurality of ~~programable~~ memory devices coupled to the embedded processor complex, wherein the plurality of memory devices ~~that~~ store a plurality of data structures that represent at least one search tree, wherein the data structures include a ~~direct~~ table comprising a plurality of entries, wherein at least one entry stores a leaf, and wherein the at least one leaf comprises a pattern corresponding to a search key containing an address~~, a pattern search control block and a leaf~~; and

~~an~~ a control memory arbiter coupled to the plurality of protocol processor, wherein the control memory arbiter ~~that~~ controls the access of each protocol processor to the plurality of

memory devices, wherein the table stored in the plurality of memory devices is utilized to match the pattern with the search key.

25. (Currently amended) The apparatus ~~fabricated on a semiconductor substrate for determining the full match~~ of claim 24 further comprising a tree search engine that operates in parallel with protocol processor execution to perform tree search instructions including memory reads and writes and memory range checking.

26. (Currently amended) The apparatus ~~fabricated on a semiconductor substrate for determining the full match~~ of claim 24 wherein the plurality of memory devices further comprises at least one of internal static random access memory, external static random access memory, and external dynamic random access memory.

27. (Currently amended) The apparatus ~~fabricated on a semiconductor substrate for determining the full match~~ of claim 24 wherein the control memory arbiter manages control memory operations by allocating memory cycles between the plurality of protocol processors and the plurality of memory devices.

28. (Currently amended) The apparatus fabricated ~~on a semiconductor substrate for determining the full match~~ of claim 24 wherein each protocol processor comprises a primary data buffer, a scratch pad data buffer and control registers for data store operations.

29. (Currently amended) The apparatus fabricated ~~on a semiconductor substrate for determining the full match~~ of claim 24 further comprising a hash box component that performs a geometric hash function on the search key.

30. (Currently amended) The apparatus ~~fabricated on a semiconductor substrate for determining the full match~~ of claim 24 further comprising a programmable search key register and a programable hashed key register.

31. (Currently amended) The apparatus ~~fabricated on a semiconductor substrate for determining the full match~~ of claim 30 further comprising a programmable color key register to enable sharing a single table data structure among a plurality of independent search trees.

32. (Currently amended) The apparatus ~~fabricated on a semiconductor substrate for determining the full match~~ of claim 31 wherein the contents of the color register, if enabled, are appended to the hash output to produce a final hashed key.

33. (Currently amended) The apparatus ~~fabricated on a semiconductor substrate for determining the full match~~ of claim 31 wherein if the color register is not enabled, appending an equivalent number of zeros to the hash output to produce a final hashed key.

34-45. (Canceled)